

# **SYSTEM AND METHOD FOR REDUCING CHARGED PARTICLE CONTAMINATION**

## **Related Applications**

- [001] This application claims benefit of U.S. provisional application serial number 60/409,919 filed at 9/10/2002.

## **Field of the invention**

- [002] The present invention relates to systems and methods for preventing charged particle (such as but not limited to ion) contamination, and especially Gallium contamination in wafers.

## **Background of the invention**

- [003] Scanning electron microscopes are known in the art. U.S. patent 5,659,172 of Wagner describes a method for reliable defect detection using multiple perspective Scanning Electron Microscope (SEM) images.
- [004] A SEM usually includes an electron gun for generating an electron beam, a SEM lens system for focusing and converging the electron beam, a deflection coil for deflecting the electron beam, a detector for detecting electrons, such as secondary emitted electron or reflected electrons that are emitted/ reflected from an inspected object and a processor that is operative to construct SEM images in response to detection signals provided from the detector.
- [005] Usually, the electron gun, the SEM lens system and the deflection coil are located within a column that is commonly referred to as SEM column. Focused ion beam (FIB) systems are known in the art. FIB systems are generally utilized to perform milling of small areas within a die, and cross sectioning. The milled or cross-sectioned area is usually analyzed to inspect pattern profiles and to detect defects. FIB systems can also be utilized to generate FIB images.

- [0006] FIB systems usually include an ion source for generating an ion beam, a FIB lens system for focusing the ion beam to provide a focused ion beam and an ion beam deflector for deflecting the focused ion beam. Typically, a broad ion beam is utilized for an initial milling step, while a narrower ion beam is utilized for a successive step of polishing the walls of the cross sectioned wafer.
- [0007] A FIB system that is operative to generate a FIB image also has a detector and a processor. Usually, the ion source, the FIB lens system and the ion beam deflector are located within a column that is commonly referred to as FIB column. The detector can also be placed within the FIB column.
- [0008] Systems that include both FIB and SEM systems are known in the art and are referred to as FIB/SEM systems. Such a system is the XL860 DualBeam Workstation of FEI.
- [0009] A common FIB ion source generates Gallium ion beams. When a focused Gallium ion beam is directed towards an area at the surface of an integrated circuit it removes a portion of that area to form a cavity defined by cavity defining walls. The Gallium ion beam also contaminates that integrated circuit, as illustrated by "Defects and Gallium – Contamination During Focused Ion Beam Micro Machining", By C. Leher, L. Frey, S. Peterson, M. Mizutani, H. Ryssel, and "Implemented gallium-ion concentrations of focused-ion beam prepared cross sections", T. Ishitani and others, 1907 Journal of Vacuum Science Technology, B 16(a), July/ August 1998.
- [0010] Some prior art methods suggest a reduction of ion contamination during the processing steps of a semiconductor. U.S patents 5306945 and 6114222 are believed to provide an adequate description of the state of the art.
- [0011] U.S patent 5306945 of Drummond suggests to reduce ion contamination by providing an integrated circuit that includes a barrier for terminating the edge of a semiconductor die. The barrier reduces contamination of the dielectric layers such as TEOS and BPSG from mobile ions which are inherent in fabrication materials. While the barrier can be formed at many points in the

die fabrication process, its formation is preferably incorporated into the Metal1 mask.

[0012] U.S. patent 6114222 of Thakur describes a method for reducing ion contamination. The method includes forming active field effect transistors in a starting substrate; forming a first insulating layer over the field effect transistor and the field oxide; forming a second insulating layer over the first insulating layer; and performing an annealing step in a nitrogen containing gas ambient prior to exposing the insulating layer to mobile ion impurities. Thakur further suggests another method to cure mobile ion contamination during semiconductor processing by annealing an insulating layer in a nitrogen containing gas ambient prior to exposing said insulating layer to mobile ion impurities.

## **Summary of the invention**

[0013] The invention provides a method for reducing ion contamination in an object, especially an integrated circuit, the ion contamination introduced by a contaminating ion beam milling step, the method includes a first step of defining a suspected ion contaminated area and a second step of removing the suspected ion contaminated area by non-contaminating removal process. Conveniently, the non-contaminating process involves directing an electron beam at the presence of an additional material, towards the object to be milled. The additional material is usually in gaseous state and can be selected from a variety of prior art materials known for enhancing or allowing milling. The additional material can be a XeF<sub>2</sub> (Xenon di-Fluoride) gas, but this is not necessarily so.

[0014] The invention provides a system for reducing ion contamination in an object, the ion contamination introduced by a contaminating ion beam milling step, the system includes means for defining a suspected ion contaminated area; and means for removing the suspected ion contaminated area by a non contaminating process.

- [0015] The invention provides a system for milling an integrated circuit, the system includes: means for fast contaminated milling of the integrated circuit, means for defining a suspected ion contaminated area, and means for non-contaminating removal of the suspected ion contaminated area. The system can also fill the decontaminated hole with a pre-selected material.
- [0016] The invention provides a method for milling an integrated circuit, the method includes: milling the integrated circuit by a fast contaminating milling process, thus introducing ion contamination, defining a suspected ion contaminated area; and removing the suspected ion contaminated area by a non contaminating process. After applying the non-contamination process, the system can cover the milled hole by an electron beam enhanced deposition of different materials, for example Silicon.
- [0017] Conveniently, the contaminating ion beam is a Gallium ion beam, while the non-contaminating removal process involves directing an electron beam to interact with additional material.
- [0018] The area may be defined in response to at least one contamination parameter. Said parameter may be (i) the area that was exposed to ion beam, (ii) at least one temperature of the integrated circuit during a time period that starts at the contaminating milling step and ends at the step of removing the suspected ion contaminated area, (iii) the time period between the contaminating ion beam milling step and the step of removing the suspected ion contaminated area, and/or (iiii) the materials from which the milled object is made of, and especially the behavior of Gallium ions within said materials. The parameter may also reflect the arrangement/ topography of said materials.
- [0019] The method can be implemented during the manufacturing of the integrated circuit, and/or during an inspection process.

## **Brief description of the drawings**

- [0020] The present invention will be more fully understood from the following detailed description of the embodiments thereof, taken together with the drawings in which:
- [0021] Figures 1a-1b are a cross sectional view and a top view of an area that includes a cavity that was formed by a contaminating milling process; Figure 2 illustrates an area after a non-contaminating removal process is implemented, in accordance with an embodiment of the invention;
- [0022] Figure 3 is an overall view of a milling system, in accordance with an embodiment of the invention; and
- [0023] Figures 4a- 4b are flow charts illustrating methods for eliminating charged particle contamination, in accordance with embodiments of the invention.

## **Detailed description of the drawings**

- [0024] It should be noted that the particular terms and expressions employed and the particular structural and operational details disclosed in the detailed description and accompanying drawings are for illustrative purposes only and are not intended to in any way limit the scope of the invention as described in the appended claims.
- [0025] The following description related to Gallium ion beams, but the invention is also applicable when handling contaminating charged particle beams.
- [0026] The invention is based on the following observations: (1) During a limited time period after a FIB was directed onto an area of a wafer, to provide a cavity defined by cavity defining walls, the Gallium ions are concentrated in close proximity to the surface of the cavity defining walls. (2) Gallium ions penetration is responsive to beam energy, the ion dose, and the time that elapsed from the formation of the cavity and is further responsive to the temperature of the cavity and of the cavity defining walls. (3) Gallium ions

may change the electrical properties of wafer elements, such as PN junctions, transistors and the like.

- [0027] Referring to the first assumption, research has shown that the most of the Gallium ions are concentrated (immediately after the cavity was formed) within few nanometers (or even tens nanometers) from the cavity defining walls. It is noted that the cavity may be several microns deep.
- [0028] Referring to the second assumption, if the Gallium contamination is not prevented or at least dramatically reduced, Gallium ions may propagate from the cavity defining walls (that are included in a non-operative die due to various factors including the cross sectioning) to other dies, thus causing other dies to malfunction.
- [0029] Furthermore, also in relation to the second assumption, a wafer usually has multiple layers and is fabricated in a multi-staged process that may include repetitive series of steps. A wafer may be cross-sectioned by FIB during the multi-staged process, either in a predefined manner, or as response to a suspected failure or defect of the wafer. At least some of the stages of wafer fabrication include subjecting the wafer to very high temperatures (hundreds and even few thousand centigrade). Thus, the Gallium ion propagation is accelerated during these heating inclusive stages.
- [0030] According to an aspect of the invention Gallium contamination is eliminated or at least substantially reduced by a non-contaminating removal step of removing a suspected contaminated area. The suspected contaminated area includes integrated circuit material, starting from the cavity defining walls, in which at least a predefined amount of Gallium ions may be located.
- [0031] The suspected contaminated area may be determined in view of measurements of previously milled integrated circuits and/or may be based on a model of Gallium contamination that takes into account ion energy and dose, the materials of the milled integrated circuit and the expected

propagation of the Gallium through them, the time period that starts from the contaminating milling step and the time of the non-contaminating removal process and the temperatures to which the cavity defining walls were subjected during that period. The length of these time period as well as the temperatures to which the object is subjected are available from the tools that are used to mill the object, and/or process it, as the manufacturing process is usually characterized by a high degree of monitoring.

- [0032] In cases where the temperatures are not measured / monitored a rough estimation can be provided, as manufacturing processes are characterized by a relatively fixed set of operations.
- [0033] Conveniently, the non-contaminating milling process is implemented by electron beams, and is performed before the milled wafer is subjected to high temperatures.
- [0034] Usually, the non-contaminating milling process is much slower than the FIB milling process, but as the non-contaminating milling process has to remove a substantially fewer amount of material from the wafer, the overall process is relatively time-efficient.
- [0035] It is noted that the non-contaminating milling process may be accelerated by injecting non-contaminating materials in the path of the electron beam being directed towards the wafer during the non-contaminating milling process.
- [0036] Referring to Figures 1a-1b illustrating a cross section view and a top view of an area 10 that includes a cavity 11 that was formed by a contaminating milling process, cavity 11 is defined by cavity defining walls 12 that are surrounded by integrated circuits 13.
- [0037] The potentially contaminated area 18 starts at the cavity defining walls and extends throughout integrated circuit 13.

- [0038] The potentially contaminated area 18 of Figure 1a-1b is determined based on the following assumptions: the contaminating milling occurred recently and that the wafer was not subjected to high temperatures since that milling.
- [0039] The depth and/or width of a cavity can range between few nanometers to few microns. Wider cavities can be inspected with a tilted electron beam, while narrow cavities may be formed for other purposes. The suspected area 18 is about 40 nanometers deep.
- [0040] Although Figures 1a-1b illustrate a vertical cavity, this is not necessarily so, as other shaped cavities may be formed. The milling process may be utilized for a preparation of TEM samples, but this is not necessarily so as the integrated circuit may be cross sectioned for imaging the cross sectioned area by other tools, including SEM, and especially SEMs that may generate an electronic beam that is oriented towards the wafer surface in an angle that differs than ninety degrees.
- [0041] Figure 2 illustrates area 11 after a non-contaminating milling process is implemented. Area 10 includes an extended cavity 22 that was formed by a contaminating milling process and the non-contaminating milling process. Extended cavity 22 includes what was previously cavity 11 and the potentially contaminated area 18. Extended cavity 22 may be larger than cavity 11 and suspected contaminated area, but this is not necessarily so.
- [0042] It is noted that the contaminating milling and the non-contaminating removal process may be implemented by FIB column and SEM column that are oriented towards each other and are focused to the same area, but may also be implemented by spaced apart FIB and FIB, as illustrated in patent application serial number 10/005190 Titled "System and method for directing a miller", filed 26 November 2001.
- [0043] Figure 3 illustrates an exemplary milling system 100, in accordance with a preferred embodiment of the invention. Milling system 100 includes SEM



110 and FIB generator 120, operative to perform contaminating milling and non-contaminating removal process, and in communication with each other to enable milling a cavity by a contaminating milling process and milling a corresponding enlarged cavity by non-contaminating milling.

[0044] SEM 110 includes a processor for defining a suspected ion contaminated area, although said processor may be located in other locations, such as within FIB generator 120, or in another remote location. The processor executes dedicated software for calculating the area and may utilize prior art models of Gallium propagation. It is noted that other hardware and/or software combination may be utilized for calculating said area. The calculation may be responsive to the topography (arrangement) of materials at the vicinity of the cavity, as well as their characteristics.

[0045] Milling system 100 further includes: (i) a controllable stage 20, for moving the inspected object from a first location in which the inspected object is accessible to the SEM 110 a second location in which the inspected object is accessible to FIB generator 120; and (ii) gas injectors 140 and 150. Gas injector 140 is located at the vicinity of the first location for providing materials to interact with an electron beam provided by SEM 110 to accelerate the non-contaminating milling, while gas injector 150 is located at the vicinity of the second location to accelerate the milling of the inspected object by the Gallium ion beam.

[0046] Figure 4a illustrates method 200 for milling an integrated circuit. Method 200 includes step 210 of milling the integrated circuit by a fast contaminating milling process, thus introducing ion contamination, step 220 of defining a suspected ion contaminated area, and step 230 of removing the suspected ion contaminated area by the non-contaminating removal process.

[0047] Figure 4b illustrates method 300 for reducing ion contamination in an object, the ion contamination introduced by a contaminating ion beam milling step, the method includes step 310 of defining a suspected ion contaminated area and

step 320 of removing the suspected ion contaminated area by the non-contaminating removal process.

[0048] It will thus be appreciated that the preferred embodiments described above are cited by way of example, and that the present invention is not limited to what has been particularly shown and described hereinabove. Rather, the scope of the present invention includes both combinations and sub-combinations of the various features described hereinabove, as well as variations and modifications thereof which would occur to persons skilled in the art upon reading the foregoing description and which are not disclosed in the prior art.